

BUDGE, William**S/N: 10/066,483****REMARKS**

Claim 24 has been amended to correct the antecedent basis issue identified by the Examiner and to clarify that the first wordline and the second wordline comprise different doping types. Claims 25 and 30 are amended to correct obvious editing errors. Claims 27 and 29 are amended to correct the claim dependencies.

The Examiner's objection to the drawings has been obviated by the proposed amendments to the drawings. The proposed amended drawings present the DRAM, SRAM, logic circuitry, and system-on-chip as a labeled rectangular box. Such depiction is in accordance with 37 C.F.R. §1.83(a) which states that "conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of ... a labeled rectangular box". The proposed amendments to the drawings are supported by the claims as originally filed and the specification and do not add any new matter.

The Examiner rejected Claims 24 and 26-31 under 35 U.S.C. §102(b) as being anticipated by USP 6,121,086 to Kuroda et al. Specifically, the Examiner refers to Figure 25 of USP'086 and identifies a P-type wordline with a first nonconductive silicon layer as #100 and an N-type wordline with a second nonconductive silicon layer as #200. The Examiner then states that the first layer is thicker than the second layer. The Applicant respectfully traverses on the grounds that the reference does not expressly or implicitly disclose all of the claim limitations and the Examiner is reading limitations from the current claims into the prior art reference.

First, the basis of the Examiner's statement regarding the relative thicknesses of the first and second nonconductive layers of #100 and #200 is unclear. The text citations provided by the

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Examiner (col. 10, line 15; col. 13, line 67; and, col. 14, line 1) are silent on the relative thicknesses of the respective nonconductive layers. Given that all of the corresponding layers of the respective wordlines were formed simultaneously, one skilled in the art would expect that all of the corresponding height thicknesses would be equal. The lateral thicknesses of the nonconductive layers in USP'086 is determined by the placement of the plugs. However, USP'086 does not seem to provide any guidance on choosing the exact plug positions. Nor can the relative layer thicknesses be deduced by an examination of the drawings. USP'086 does not teach that the figures are to scale, and, therefore, any conclusions drawn from a comparison of the drawings is speculative, at best.

Second, if the Examiner is relying on inherency to imply the missing thickness relationships, then the Examiner must provide reasoning for why the claimed relationship must necessarily and inevitably result from the teaching of USP'086. The Examiner has not provided such reasoning.

Therefore, the anticipation rejection of Claim 24, and all claims dependent therefrom, fails because the Examiner has failed to show that USP'086 discloses all elements of the current claims.

The Examiner rejected Claim 25 under 35 U.S.C. §103(a) as being unpatentable over USP 6,121,086. The Applicants traverse this rejection on the grounds that USP'086 fails to teach all elements of the claimed invention as argued above (above arguments incorporated here by reference). Therefore, the *prima facie* case fails and should be withdrawn.

An IDS was submitted at the time the application was filed but the Examiner has not returned an initialed copy of the PTO-1449. The Examiner is requested to indicate that the references of the IDS have been considered.

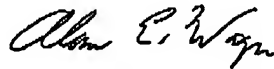
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The Applicants believe that the above amendments and remarks place the application in condition for allowance. Therefore, the Applicants request that the Examiner issue a Notice of Allowance for Claims 24-31.

Respectfully submitted,



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